Abstract of the Invention

The invention provides an embedded processor architecture comprising a plurality of virtual processing units that each execute processes or threads (collectively, "threads"). One or more execution units, which are shared by the processing units, execute instructions from the threads. An event delivery mechanism delivers events — such as, by way of non-limiting example, hardware interrupts, software-initiated signaling events ("software events") and memory events — to respective threads without execution of instructions. Each event can, per aspects of the invention, be processed by the respective thread without execution of instructions outside that thread. The threads need not be constrained to execute on the same respective processing units during the lives of those threads — though, in some embodiments, they can be so constrained. The execution units execute instructions from the threads without needing to know what threads those instructions are from. A pipeline control unit which launches instructions from plural threads for concurrent execution on plural execution units.